CLAIMS:

1. A clock distribution circuit comprising:

a clock source to generate a clock signal;

a clock divider to divide the clock signal and produce a divided clock signal, and including a flip-flop that introduces a first propagation delay to the divided clock signal; and

a delay matching circuit to distribute the clock signal, and to introduce a second propagation delay to the clock signal, the second propagation delay substantially matching the first propagation delay introduced in the divided clock signal by the flip-flop.

2. The circuit of claim 1, wherein the delay matching circuit includes:

a multiplexer having a select line coupled to a clock source;

transmission gates within the multiplexer to substantially mimic characteristics of a slave transmission gate in a flip-flop;

inputs coupled to the multiplexer to substantially mimic characteristics of a master output driver of the flip-flop; and

an output coupled to the multiplexer to substantially mimic characteristics an output driver in the flip flop.

3. The circuit of claim 1, wherein the delay matching circuit substantially mimics current signal and current sourcing characteristics of the flip-flop.

4. The circuit of claim 1, wherein the delay matching circuit substantially mimics output drive characteristics of the flip-flop.

5. The circuit of claim 1, wherein the first propagation delay is a clock-to-Q propagation delay.

6. The circuit of claim 1, wherein the delay matching circuit includes a multiplexer, the multiplexer including a select line coupled to the clock source.

7. The circuit of claim 1, wherein the delay matching circuit includes a multiplexer having a first input coupled to drive a first transmission gate, a second input coupled to drive a second transmission gate, a select input coupled to the clock source to selectively enable one of the transmission gates, and an output coupled to the first and second transmission gates, wherein the transmission gates are configured to correspond substantially to a slave transmission gate in the flip-flop.

8. The circuit of claim 7, wherein the transmission gates are configured to correspond substantially in size to the slave transmission gate in the flip-flop.

9. The circuit of claim 7, wherein the delay matching circuit includes:

a PMOS transistor having a drain coupled to the first input, a gate coupled to ground, and a source coupled to a supply voltage, wherein the PMOS transistor is configured to correspond substantially to a PMOS transistor in a master output driver of the flip-flop; and

an NMOS transistor having a drain coupled to the second input, a gate coupled to the supply voltage, and a source coupled to ground, wherein the NMOS transistor is configured to correspond substantially to an NMOS transistor in the master output driver of the flip-flop.

10. The circuit of claim 9, wherein the PMOS transistor is configured to correspond substantially in size to the PMOS transistor in the master output driver of the flip-flop, and the NMOS transistor is configured to correspond substantially in size to the NMOS transistor in the master output driver of the flip-flop.

11. The circuit of claim 7, wherein the delay matching circuit includes an inverter coupled to the output of the multiplexer, wherein the inverter is configured to correspond substantially to an output driver in the flip flop.

12. The circuit of claim 1, wherein the delay matching circuit includes:

means for mimicking characteristics of slave transmission gates in the flip-flop;

means for mimicking characteristics of transistors in a master output driver of the flip-flop; and

means for mimic characteristics of an output driver in the flip-flop.

13. The circuit of claim 1, wherein the clock divider includes a first asynchronous reset feature, and the delay matching circuit includes a second asynchronous reset feature that mimics operation of the first asynchronous reset feature.

14. A delay matching circuit comprising:

a multiplexer coupled to a clock source;

transmission gates within the multiplexer to substantially mimic characteristics of a slave transmission gate in a flip-flop;

inputs coupled to the multiplexer to substantially mimic characteristics of a master output driver of the flip-flop; and

an output coupled to the multiplexer to substantially mimic characteristics an output driver in the flip flop.

15. The circuit of claim 14, wherein the inputs include a first input coupled to drive a first transmission gate, and a second input coupled to drive a second transmission gate, the multiplexer further including a select input coupled to the clock source to selectively enable one of the transmission gates, wherein the output is coupled to the first and second transmission gates, and the transmission gates are configured to correspond substantially to slave transmission gates in a flip-flop.

16. The circuit of claim 14, further comprising:

a PMOS transistor having a drain coupled to the first input, a gate coupled to ground, and a source coupled to a supply voltage, wherein the PMOS transistor is configured to correspond substantially to a PMOS transistor in a master output driver of the flip-flop; and

an NMOS transistor having a drain coupled to the second input, a gate coupled to the supply voltage, and a source coupled to ground, wherein the NMOS transistor is configured to correspond substantially to an NMOS transistor in the master output driver of the flip-flop.

17. The circuit of claim 14, further comprising an inverter coupled to the output of the multiplexer, wherein the inverter is configured to correspond substantially to an output driver in the flip flop.

18. The circuit of claim 14, wherein the first propagation delay is a clock-to-Q propagation delay.

19. The circuit of claim 14, further comprising an asynchronous reset feature to permit asynchronous reset of the output independently of a clock signal generated by the clock source.

20. A delay matching circuit comprising:

a multiplexer having a first input coupled to drive a first transmission gate, a second input coupled to drive a second transmission gate, a select input coupled to a clock source to selectively enable one of the transmission gates, and an output coupled to the first and second transmission gates, wherein the transmission gates are configured to correspond substantially to a slave transmission gate in a flip-flop;

a PMOS transistor having a drain coupled to the first input, a gate coupled to ground, and a source coupled to a supply voltage, wherein the PMOS transistor is configured to correspond substantially to a PMOS transistor in a master output driver of the flip-flop;

an NMOS transistor having a drain coupled to the second input, a gate coupled to the supply voltage, and a source coupled to ground, wherein the NMOS transistor is configured to correspond substantially to an NMOS transistor in the master output driver of the flip-flop;

an inverter coupled to the output of the multiplexer, wherein the inverter is configured to correspond substantially to an output driver in the flip flop.

21. A circuit comprising:

a signal source to generate a signal;

a signal distribution circuit to modify the signal and distribute a modified signal, and including a flip-flop that introduces a first propagation delay in the modified signal; and

a delay matching circuit to distribute the signal, and introduce a second propagation delay to the signal, the second propagation delay substantially matching the first propagation delay introduced in the modified signal by the flip-flop.

22. The circuit of claim 21, wherein the delay matching circuit includes:

a multiplexer having a select line coupled to a signal source;

transmission gates within the multiplexer to substantially mimic characteristics of a slave transmission gate in a flip-flop;

inputs coupled to the multiplexer to substantially mimic characteristics of a master output driver of the flip-flop; and

an output coupled to the multiplexer to substantially mimic characteristics an output driver in the flip flop.

23. The circuit of claim 21, wherein the delay matching circuit includes a multiplexer having a first input coupled to drive a first transmission gate, a second input coupled to drive a second transmission gate, a select input coupled to the signal source to selectively enable one of the transmission gates, and an output coupled to the first and second transmission gates, wherein the transmission gates are configured to correspond substantially to a slave transmission gate in the flip-flop.

24. The circuit of claim 23, wherein the transmission gates are configured to correspond substantially in size to the slave transmission gate in the flip-flop.

25. The circuit of claim 23, wherein the delay matching circuit includes:

a PMOS transistor having a drain coupled to the first input, a gate coupled to ground, and a source coupled to a supply voltage, wherein the PMOS transistor is configured to correspond substantially to a PMOS transistor in a master output driver of the flip-flop; and

an NMOS transistor having a drain coupled to the second input, a gate coupled to the supply voltage, and a source coupled to ground, wherein the NMOS transistor is configured to correspond substantially to an NMOS transistor in the master output driver of the flip-flop.

26. The circuit of claim 25, wherein the PMOS transistor is configured to correspond substantially in size to the PMOS transistor in the master output driver of the flip-flop, and the NMOS transistor is configured to correspond substantially in size to the NMOS transistor in the master output driver of the flip-flop.

27. The circuit of claim 23, wherein the delay matching circuit includes an inverter coupled to the output of the multiplexer, wherein the inverter is configured to correspond substantially to an output driver in the flip flop.

28. A method comprising:

dividing a clock signal with a flip-flop to produce a divided clock signal, and to introduce a first propagation delay to the divided clock signal; and

introducing a second propagation delay to the clock signal with a delay matching circuit, the second propagation delay substantially matching the first propagation delay introduced in the divided clock signal by the flip-flop, wherein the delay matching circuit substantially mimics delay characteristics of the flip-flop.

29. The method of claim 28, wherein the delay matching circuit includes:

a multiplexer having a select line coupled to a clock source;

transmission gates within the multiplexer to substantially mimic characteristics of a slave transmission gate in a flip-flop;

inputs coupled to the multiplexer to substantially mimic characteristics of a master output driver of the flip-flop; and

an output coupled to the multiplexer to substantially mimic characteristics an output driver in the flip flop.

30. The method of claim 28, wherein the first propagation delay is a clock-to-Q propagation delay.

31. The method of claim 28, wherein the delay matching circuit includes a multiplexer having a first input coupled to drive a first transmission gate, a second input coupled to drive a second transmission gate, a select input coupled to the clock source to selectively enable one of the transmission gates, and an output coupled to the first and second transmission gates, wherein the transmission gates are configured to correspond substantially to slave transmission gates in the flip-flop.

32. The method of claim 31, wherein the delay matching circuit includes:

a PMOS transistor having a drain coupled to the first input, a gate coupled to ground, and a source coupled to a supply voltage, wherein the PMOS transistor is configured to correspond substantially to a PMOS transistor in a master output driver of the flip-flop; and

an NMOS transistor having a drain coupled to the second input, a gate coupled to the supply voltage, and a source coupled to ground, wherein the NMOS transistor is configured to correspond substantially to an NMOS transistor in the master output driver of the flip-flop.

33. The method of claim 31, wherein the delay matching circuit includes an inverter coupled to the output of the multiplexer, wherein the inverter is configured to correspond substantially to an output driver in the flip flop.